WHAT IS CLAIMED IS:

1. A memory device, comprising:

a memory cell configured to be coupled to complementary first and second bit lines;

a differential amplifier having first and second input terminals and operative to amplify a voltage between the first and second input terminals to produce an output signal;

first and second voltage-dependent capacitors coupled to respective ones of the first and second input terminals; and

first and second switches operative to couple and decouple the first and second bit lines to and from respective ones of the first and second voltage-dependent capacitors.

2. A device according to Claim 1, wherein the first and second switches comprise respective first and second isolation transistors.

3. A device according to Claim 2, wherein the first and second isolation switches comprise respective first and second NMOS transistors.

4. A device according to Claim 1, wherein the first and second voltage-dependent capacitors comprise respective MOS capacitors.

5. A device according to Claim 1, wherein the differential amplifier comprises:

first and second output terminals;

first and second conductors that couple respective ones of the first and second input terminals to respective ones of the first and second output terminals;

a first circuit operative to drive one of the first and second conductors to a signal ground based on voltages at the first and second input terminals responsive to a first control signal; and

a second circuit operative to drive one of the first and second conductors to a power supply voltage based on voltages at the first and second input terminals responsive to a second control signal.

6. A device according to Claim 5:

wherein the first circuit comprises:

a first NMOS transistor having a drain coupled to the first conductor and a gate coupled to the second conductor;

a second NMOS transistor having a drain couple to the second conductor, a gate coupled to the first conductor, and a source coupled to a source of the first NMOS transistor and configured to receive the first control signal;

wherein the second circuit comprises:

a first PMOS transistor having a drain coupled to the first conductor and a gate coupled to the second conductor; and

a second PMOS transistor having a drain couple to the second conductor, a gate coupled to the first conductor, and a source coupled to a source of the first PMOS transistor and configured to receive the second control signal.

7. A sense amplifier, comprising:

a differential amplifier having first and second input terminals and operative to amplify a voltage between the first and second input terminals to produce an output signal;

first and second voltage-dependent capacitors coupled to respective ones of the first and second input terminals; and

first and second switches operative to couple and decouple first and second bit lines to and from respective ones of the first and second voltage-dependent capacitors.

8. A sense amplifier according to Claim 7, wherein the first and second switches comprise respective first and second isolation transistors.

9. A sense amplifier according to Claim 8, wherein the first and second isolation switches comprise respective first and second NMOS transistors.

10. A sense amplifier according to Claim 7, wherein the first and second voltage-dependent capacitors comprise respective MOS capacitors.

11. A sense amplifier according to Claim 7, wherein the differential amplifier comprises:

first and second output terminals;

first and second conductors that couple respective ones of the first and second input terminals to respective ones of the first and second output terminals;

a first circuit operative to drive one of the first and second conductors to a signal ground based on voltages at the first and second input terminals responsive to a first control signal; and

a second circuit operative to drive one of the first and second conductors to a power supply voltage based on voltages at the first and second input terminals responsive to a second control signal.

12. A sense amplifier according to Claim 11:

wherein the first circuit comprises:

a first NMOS transistor having a drain coupled to the first conductor and a gate coupled to the second conductor;

a second NMOS transistor having a drain couple to the second conductor, a gate coupled to the first conductor, and a source coupled to a source of the first NMOS transistor and configured to receive the first control signal;

wherein the second circuit comprises:

a first PMOS transistor having a drain coupled to the first conductor and a gate coupled to the second conductor;

a second PMOS transistor having a drain couple to the second conductor, a gate coupled to the first conductor, and a source coupled to a source of the first PMOS transistor and configured to receive the second control signal.

13. A method of operating a memory device, the method comprising:

coupling respective terminals of first and second voltage-dependent capacitors to respective ones of complementary first and second bit lines to develop a voltage difference between the terminals of the first and second voltage-dependent capacitors responsive to data stored in a memory cell couple to the first and second bit lines;

decoupling the first and second bit lines from the terminals of the first and second voltage-dependent capacitors to increase the voltage difference between the terminals of the first and second voltage-dependent capacitors; and

amplifying the increased voltage difference to generate an output signal indicative of the data stored in the memory cell.

14. A method according to Claim 13, wherein the first and second voltage-dependent capacitors comprise respective MOS capacitors.

15. A method according to Claim 13:

wherein coupling terminals of first and second voltage-dependent capacitors to respective ones of complementary first and second bit lines comprises turning on respective first and second isolation transistors to couple the terminals of the first and second voltage-dependent capacitors to respective ones of the first and second bit lines; and

wherein decoupling the first and second bit lines from the terminals of the first and second voltage-dependent capacitors comprises turning off the first and second isolation transistors.

16. A method according to Claim 13, wherein amplifying the increased voltage difference comprises:

applying the increased voltage difference to a differential amplifier; and

activating the differential amplifier to generate the output signal.